Small-Signal Substrate Resistance Effect in RF CMOS Cascode Amplifier

Choong-Yul Cha, Jin-Pil Kim, and Sang-Gug Lee

***Abstract*—With common-source RF application amplifier, it is well known that the small substrate resistance helps to improve the output resistance as well as the transconductance. This idea can be easily extended to all CMOS transistors in RF applications. However, with cascode amplifier at high frequencies, the maximum available gain, noise figure minimum, and the tuned output impedance are improved by increasing the substrate resistance of the common-gate transistor, so that the range of operational frequency can be extended. These contradicting phenomenons between the common-source and common-gate topology can be explained theoretically, and the supporting measurement results are presented base on a 0.35 μm CMOS technology.**

***Index Terms*—Cascode amplifier, CMOS, maximum available gain, RF, substrate resistance.**

I. Introduction

WIRELESS communications at GHz frequencies are a huge market that drives the semiconductor technology toward low-cost solutions. CMOS technology is an attractive solution due to the low cost, high level integration, and even high performance in terms of cutoff frequency [1], [2]. Many existing wireless systems operate around 2 GHz band with the data rates below 2 Mbps. As the mobile data service evolves to the multimedia service, the frequency band of operation must go up to meet the higher data-rate. For this reason, 5 GHz ranges are expected to be a widely used frequency bands for the next generation multimedia mobile services [3].

In CMOS technology, as the operation frequency goes up, the substrate parasitic impedance, which exists between drain/source node and ground, critically affects the RF performance of the transistor. With common-source amplifier, high substrate resistance lowers the output resistance and transconductance. The well-known method to minimize substrate effect is to reduce the substrate resistance by placing substrate contacts around the MOSFET [4]–[8].

This paper presents that the high frequency characteristics improve with higher substrate resistance in common-gate topology when the input is driven by a current source. Therefore, with cascode amplifier, the high frequencies characteristics such as the maximum available gain, minimum noise figure, and tuned output impedance improve considerably. The enhanced cascode amplifier performances allow the given technology more useful at higher frequencies. Cascode amplifiers are fabricated based on 0.35 μm CMOS technology and demonstrated that the higher substrate resistance on common-gate transistor improves performance over the frequency band of 2 to 10 GHz. The proposed variation can extend the 0.35 μm technology potential to the 5 GHz applications.

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The authors are with the Information and Communications University, Daejeon 305-732, Korea (e-mail: netcar@icu.ac.kr).

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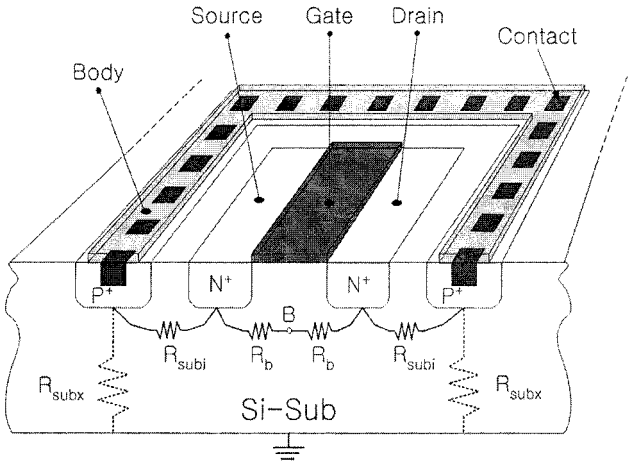

Fig. 1. Cross section of an RF CMOS transistor showing the corresponding parasitic resistances.

II. Substrate Resistance Effect in CMOS Amplifier—Theory and Measurement

Fig. 1 shows the cross section of an RF CMOS transistor with parasitic substrate resistances. In Fig. 1, R_b, R_{subi}, and R_{subx} represent the effective body, intrinsic substrate, and the extrinsic substrate resistances, respectively [4]–[6]. Fig. 2 shows a cascode amplifier topology with parasitics relevant to the discussions of this paper. In Fig. 2, C_{jd} and C_{js} are the drain-to-substrate and source-to-substrate junction capacitances, C_{gs} the gate-to-source capacitance, and R_b the effective body resistance, respectively. With transistor M_1 in Fig. 2, the body terminal is shorted to source, while with M_2, the body terminal has the option of either being grounded or left open (note the switch).

With common-source amplifiers, it is well known that reducing substrate resistance ($R_{sub} = R_{subi} + R_{subx}$) helps to improve the high frequency performances such as trasconductance and output impedance. The improvement in transconductance can be explained using the common-source part of the schematic shown in Fig. 2. Assuming that a high impedance load terminates the drain node of the common-source transistor, a signal applied at the gate of common-source will generate a large inverted voltage swing at the drain node. At high frequencies, the feed-through of the large output voltage swing through C_{jd1} generates a voltage swing at the body node (B_1 in Fig. 2). The

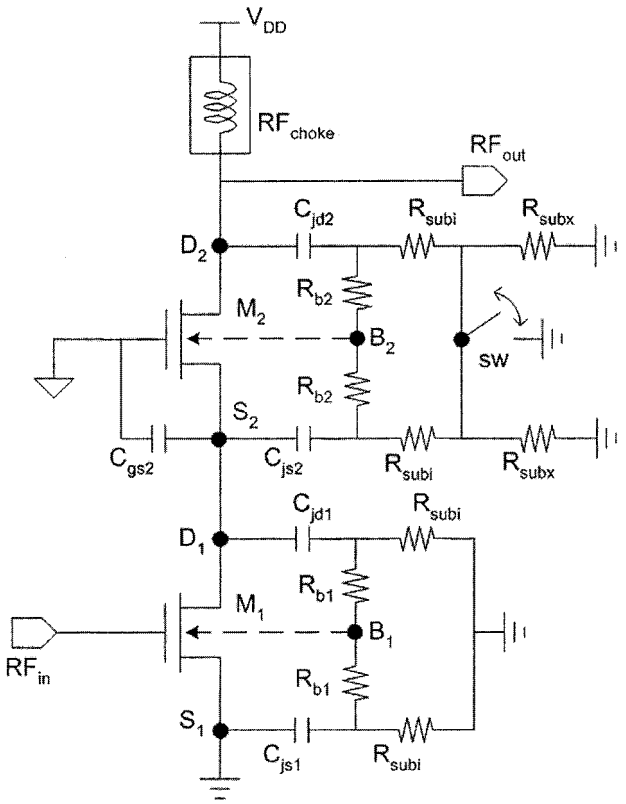

Fig. 2. Cascode amplifier with substrate parasitics.

applied signal at the gate and the induced signal at the body node are out of phase, leading to overall transconductance degradation. Similarly, the output impedance degradation can also be explained by the feedback mechanism. Therefore, by minimizing the R_{sub}, the RF performances of the common-source topology can be improved. RF IC designers tend to minimize R_{sub} by placing multiple substrate contacts surrounding CMOS transistor, as shown in Fig. 1, and the body terminal is connected to the nearest grounds. This minimizes R_{subi} and removes R_{subx}.

However, with the common-gate stage in the cascode amplifier the situation can be different. Note that the source node of common-gate stage is driven by a current source. From Fig. 2 and assuming high impedance loading at the drain node of M_2, the input current at the source of M_2 will generate a large in-phase output voltage swing. At high frequencies, the output voltage signal can be feed to the body (B_2) and source (S_2) nodes of M_2 through the parasitic capacitors C_{jd2} and C_{js2}. With small R_{sub}, compare to the impedances of C_{jd2} and C_{js2}, the feed-through effects are negligible. However, by increasing R_{sub} (for example, open the switch), the amount of feedback can increase. As an extreme case, assuming $R_{b2}s$ are small enough to neglect, if $R_{subi} + R_{subx} \gg 1/sC_{jd2}(= 1/sC_{js2})$, the parasitic capacitors C_{jd2}, C_{js2}, and C_{gs2} forms a capacitive voltage divider network. Typically, R_bs are small [6] and $C_{jd}(= C_{js})$ is about 30–40% of C_{gs}. Therefore, the large output voltage swing introduces feedback voltages at the body (B_2) and source (S_2) nodes. The voltage drop across body-to-source provides negative feedback to the output, while the source-to-gate voltage leads to positive feedback to the

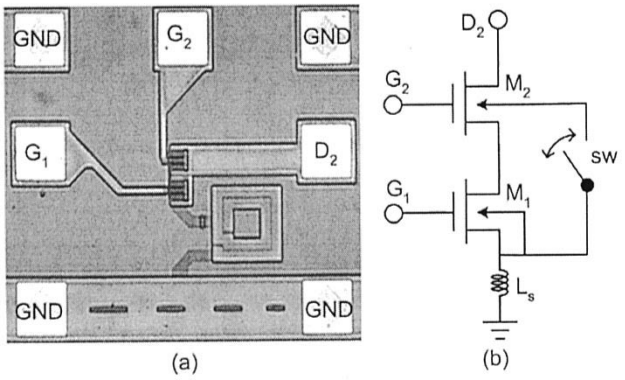

Fig. 3. (a) Microphotograph of the cascode amplifier with degeneration inductor and (b) the corresponding circuit schematic.

output. Considering the capacitor size ratio (C_{gs}, C_{jd}, and C_{js}) and the fact that the transconductance of MOS transistor is 4 to 10 times more sensitive on the gate-source voltage than that of the body-source voltage [9], the effect of positive feedback dominates compare to that of the negative feedback leading to higher output voltage swing. Another way to look at this phenomenon is that in Fig. 2, C_{jd2}, C_{js2}, C_{gs2}, and M_2 constitutes an oscillator topology with inductive termination at the output [10]. The combination of C_{jd2}, C_{js2}, C_{gs2}, and M_2 provide negative resistance at the drain node of M_2. This means the increase in the quality factor of the output impedance, which leads to increase in the tuned output impedance and maximum available gain for the cascode amplifier at high frequencies. Note that the larger the value of R_{sub} the lower the frequency where the positive feedback kicks in. In addition, the large value of R_{sub} in the common-gate transistor provides higher parasitic substrate impedance seen from the source node of M_2 to ground. The higher substrate impedance at the source node of M_2 helps to suppress the noise contribution of M_2 to the output, leading to lower overall minimum noise figure of the cascade amplifier [11].

A simple cascode amplifier with inductive source degeneration is fabricated, which is configured to experiment the small-signal substrate resistance effect at high frequencies based on a 0.35 μm epi-CMOS technology. Fig. 3 shows the microphotograph of the cascode amplifier and the corresponding circuit schematic where the transistor of 0.35×200 μm size is used and a 2 nH inductor for the degeneration. In Fig. 3, the inductor is added considering typical low noise amplifier topology where degeneration helps to achieve simultaneous gain and noise matching. As shown in Fig. 3(b), the body node of the common-gate is configured in two different ways: (i) the body node of common-gate is shorted to that of the common-source transistor by metal (ii) the body node of common-gate is floated from the external ground except through the silicon substrate. Note that with case (ii), the substrate resistance of common-gate transistor is $(R_{subi} + R_{subx})/2$.

Fig. 4 compares the maximum available gain of the two different configurations based on the simulated and measured S-parameters. In the simulation, the transistor model predicted the small-signal parasitic capacitances of $C_{jd} = 85$ fF, $C_{js} = 97.6$ fF, and $C_{gs} = 272$ fF, respectively, with the common-gate transistor. The small-signal transistor model

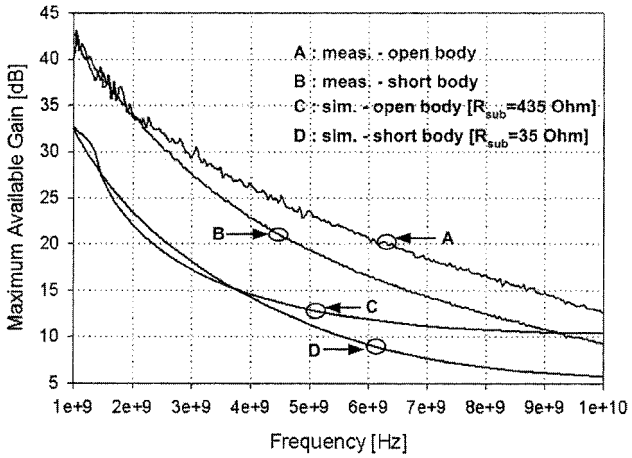

Fig. 4. Maximum available gain of the two different cascode configurations, short and open body, based on the simulated and measured S-parameters.

within the commercial simulator, which is used in this work, assumes $R_b = 0$ [5]. Therefore, the substrate resistances are added as a single resistor connected from the node B_2 to ground (see Fig. 2). Since the exact values of the substrate resistances are difficult to extract, $R_{sub} = (R_{subi} + R_{subx})/2$ of 435 and 35 Ω are used for the simulation. As can be seen from Fig. 4, at high frequencies, both the measurement and simulation show the increase in the maximum available gain with higher substrate resistance in common-gate transistor. The overall shift in the simulated result compare to that of the measurement might have been caused by the inaccuracies in the small-signal model as well as the model parameter values. However, the overall frequency behavior agrees well with the measurement. In Fig. 4, from the measurement, at frequencies above 2 GHz, the floated-body common-gate cascode amplifier starts to show higher maximum available gain. At frequencies near 5 GHz, the difference of the measured maximum available gains is about 4.5 dB.

III. Conclusions

The small-signal substrate resistance effect in RF CMOS cascode amplifier has been investigated. For common-source amplifier, the output feed-through to the body node can degrade the output resistance and transconductance considerably. Therefore, the substrate resistance should be minimized. However, in cascode amplifier at high frequencies, the maximum available gain, tuned output impedance, and minimum noise figure gets improved when the substrate resistance of the common-gate transistor is maximized. The enhanced cascode amplifier performances allow the given technology more useful at higher frequencies. The enhancement of the power gain is explained by identifying the resulting oscillator configuration of the common-gate topology at high frequencies. Higher substrate resistance of the common-gate stage helps to reduce the minimum noise figure of the cascode amplifier as well. A simple cascode amplifier with inductive degeneration is fabricated for the verification based on a 0.35 μm CMOS technology, and demonstrated the improvements in the maximum available gain at frequencies higher than 2 GHz by increasing substrate resistance of the common-gate transistor. An equivalent circuit simulation predicted the same trend.

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